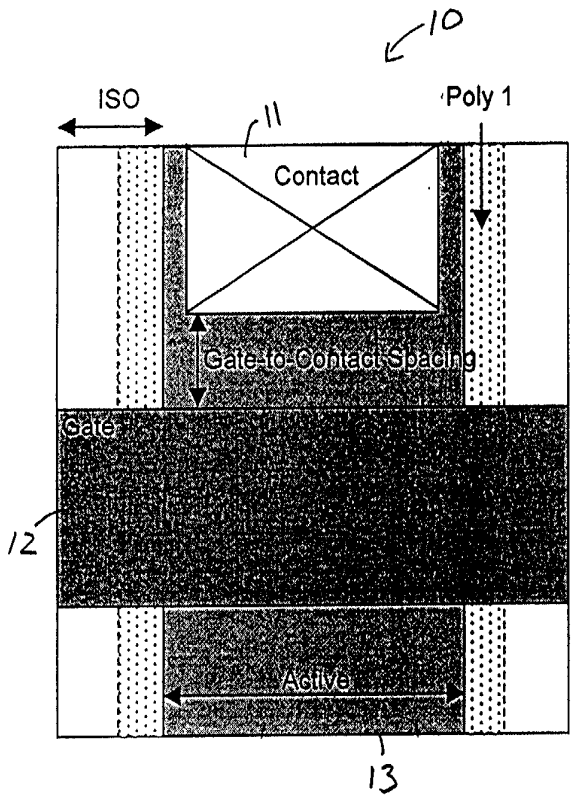

FIG. 1A (Prior Art)

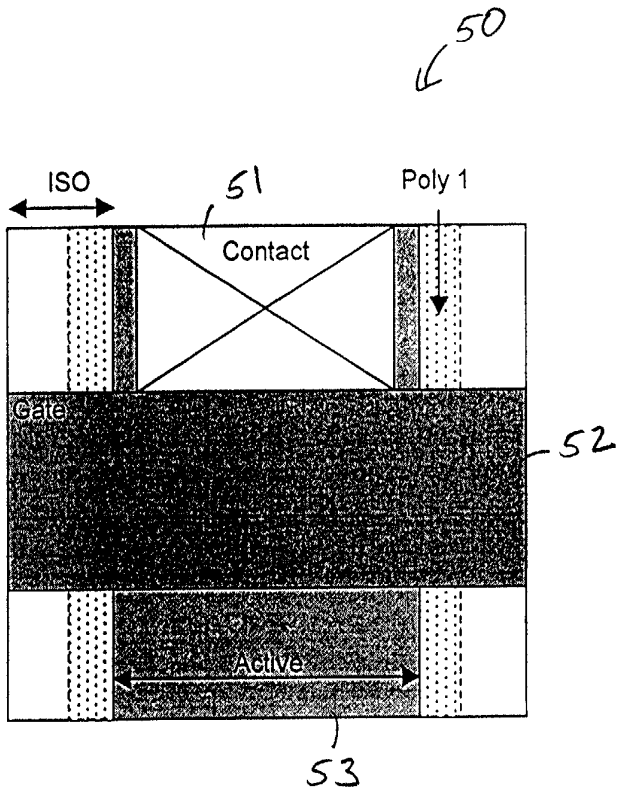

FIG. 1B

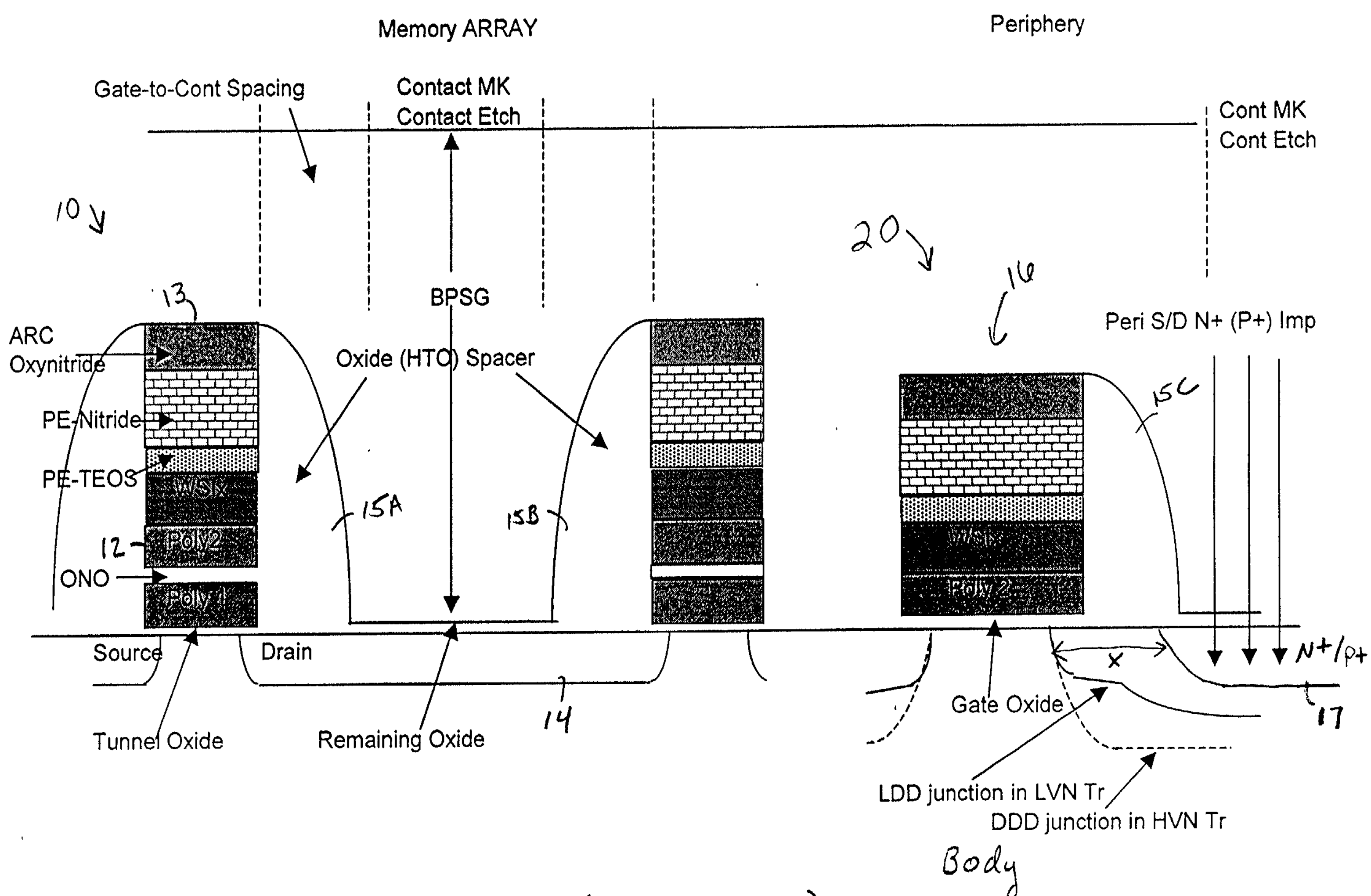

FIG. 2 (Prior Art)

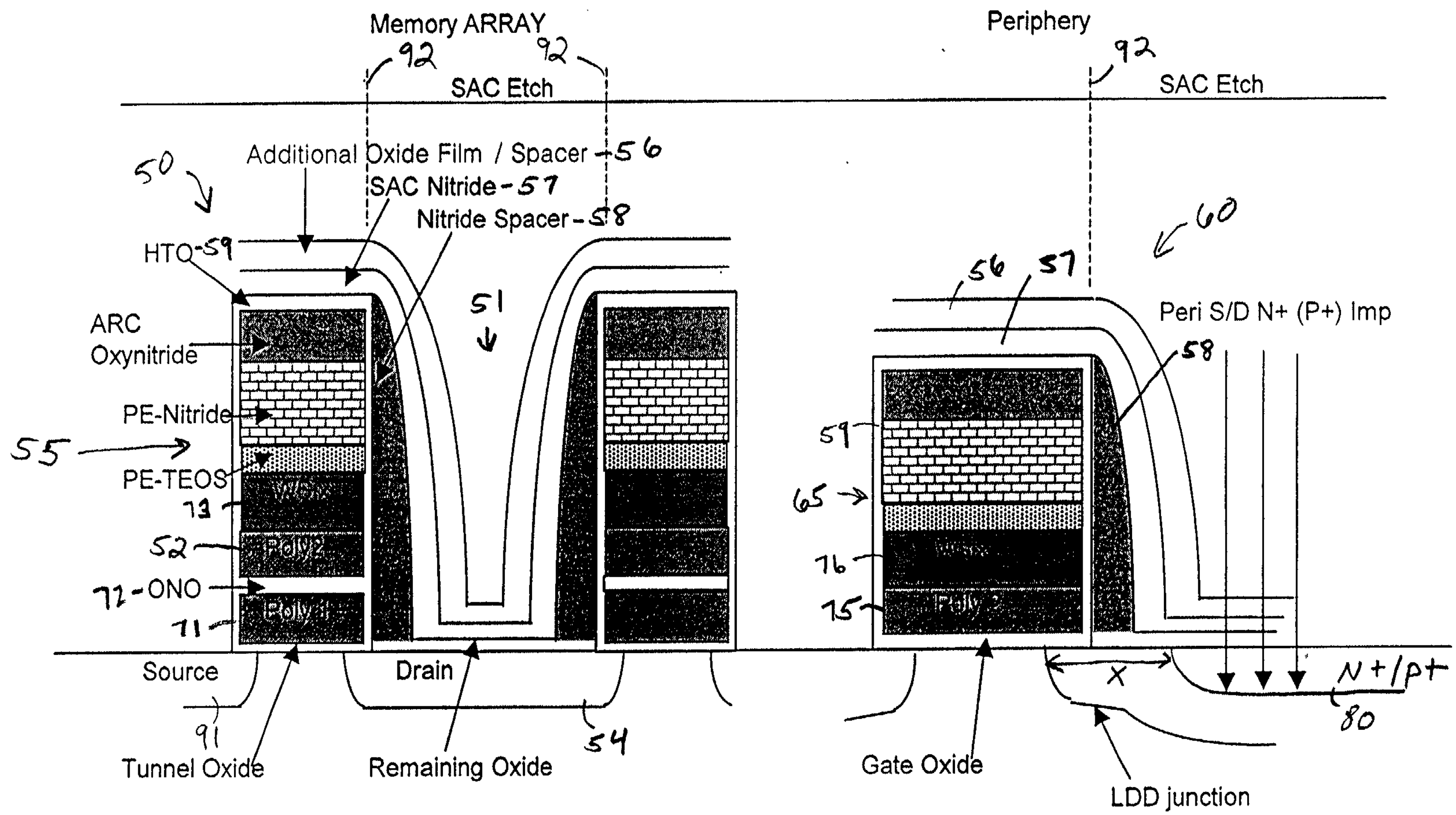

FIG. 3

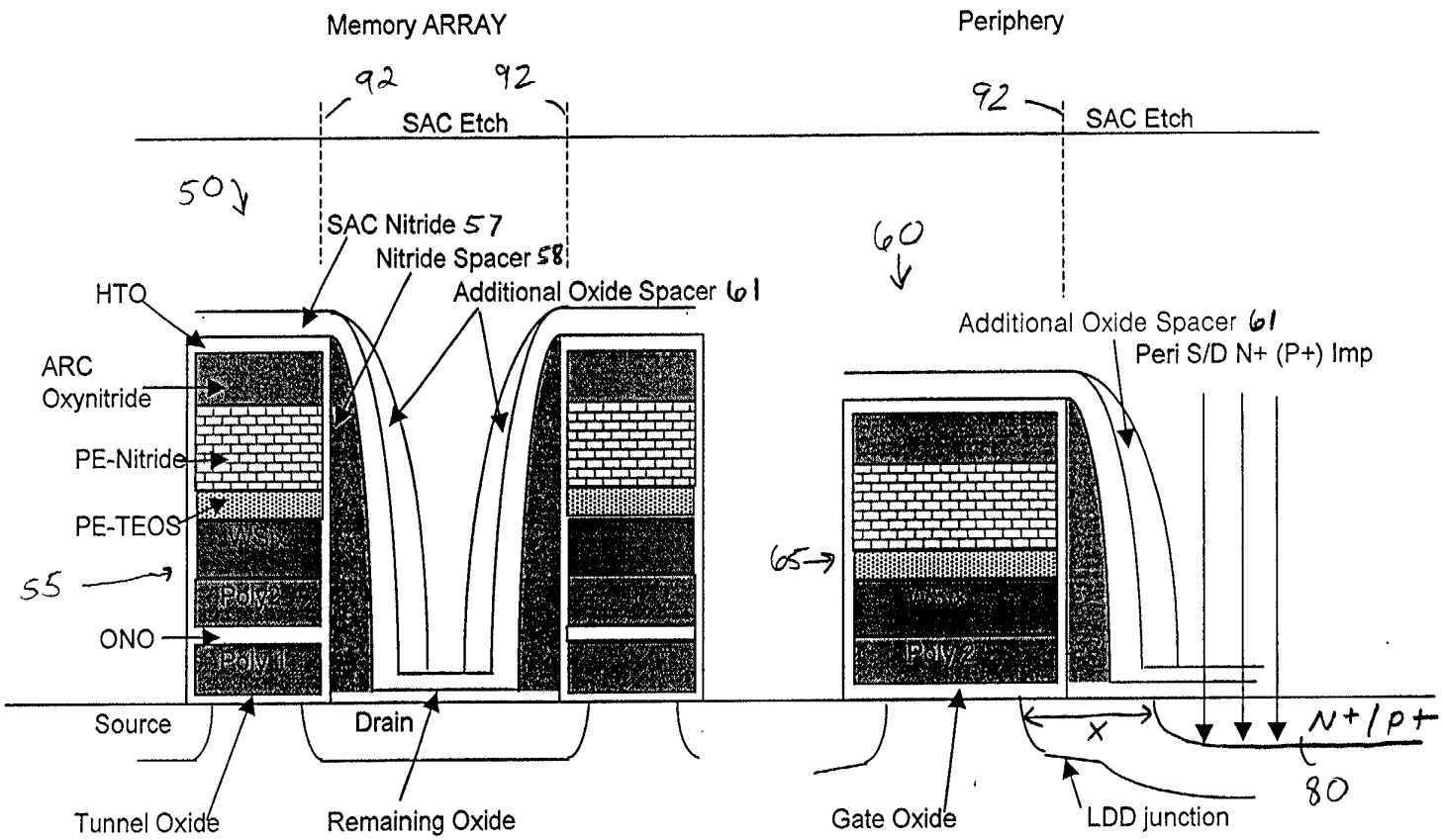
Memory ARRAY
Periphery
92
92
92
SAC Etch
SAC Etch
50
SAC Nitride 57
Nitride Spacer 58
Additional Oxide Spacer 61
60
HTO
ARC
Oxynitride
PE-Nitride
PE-TEOS
55
ONO
Poly2
Poly1
Additional Oxide Spacer 61
Peri S/D N+ (P+) Imp
65
Poly2
Source
Drain
X
N+/P+
80
Tunnel Oxide
Remaining Oxide
Gate Oxide
LDD junction

FIG. 4